Wide-Tuning Range Si Bipolar VCO's Based on Three-Dimensional MMIC Technology

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***Abstract*— The first completely integrated silicon (Si) bipolar junction transistor (BJT) voltage-controlled oscillators (VCO's), based on three-dimensional (3-D) monolithic-microwave integrated-circuit (MMIC) technology are presented in this paper. The 3-D MMIC technology offers the use of reactive matching in circuit design as well as GaAs MMIC construction and expands the operation frequency of Si MMIC's. Two types of VCO MMIC's using 0.5-μm Si BJT's are presented and demonstrated. Both exhibit a very wide frequency tuning range in the 5- and 6-GHz bands. The former offers the frequency tuning range of 33% using the base–emitter conductance operation of the BJT, which works like a varistor with a large ratio. Furthermore, the oscillation frequency is remarkably linear against the controlled base bias. To confirm the wide-tuning ability of the proposed VCO at higher frequencies, a 7-GHz-band VCO is fabricated on the same Si masterslice array used for the 5-GHz-band VCO. It achieves a 28% tuning range from 5.53 to 7.09 GHz at the collector bias of 2 V. The latter, whose frequency is controlled by a varactor diode, also offers a wide tuning range from 5.15 to 6.75 GHz. The phase noise achieved ranges from -95 dBc/Hz to -117 dBc/Hz at 1-MHz offset frequency over the tuning range of 1.6 GHz (best phase noise performance is -90.5 dBc/Hz at 100 kHz). Measured results show that 3-D MMIC Si VCO's can be developed that yield frequencies above 7 GHz.**

***Index Terms*— Masterslice, microwave bipolar transistor, MMIC, oscillator, three-dimensional, VCO.**

I. Introduction

RECENTLY, the demand for millimeter-wave and monolithic microwave integrated circuits (MMIC's) has been continuously growing to realize the multimedia era. Cost is the most important issue in developing MMIC's. A low-cost low phase-noise oscillator with wide tuning range is urgently needed as the local oscillators in microwave and millimeter-wave systems. Silicon (Si) bipolar junction transistors (BJT's) are considered excellent candidates for cost-effective and low phase-noise voltage-controlled oscillator (VCO) applications because they offer lower $1/f$ noise than MESFET's and high electron-mobility transistors (HEMT's). Several monolithic Si VCO's have been recently reported [1]–[3]. However, few papers have demonstrated Si VCO MMIC's for frequencies above 5 GHz due to the loss of the Si substrate.

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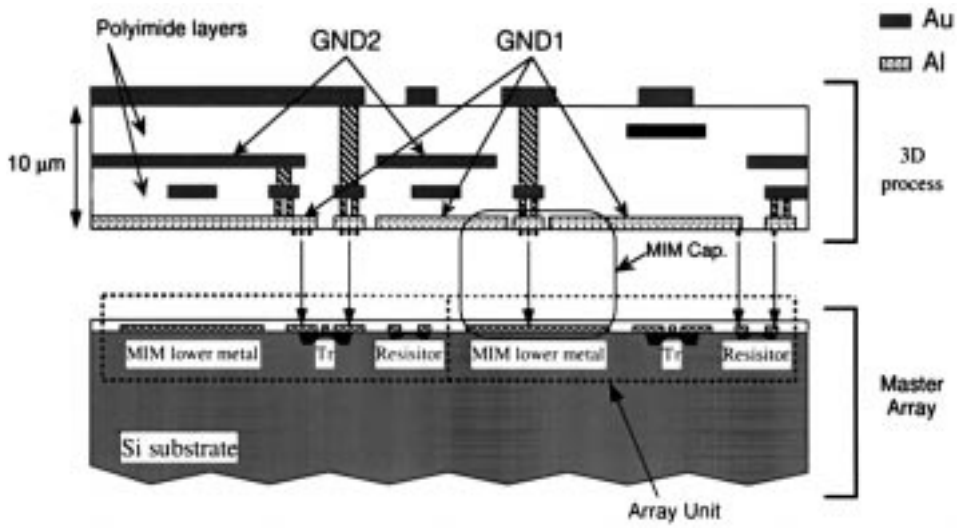
Three-dimensional (3-D) MMIC technology [4]–[7] has the potential to solve this problem. This is because 3-D MMIC's can provide passive circuits that are shielded from the effects of the lossy Si substrate. In addition, 3-D MMIC technology can expand the application region of Si devices to higher frequencies by using reactive matching, as is possible with GaAs MMIC's. Furthermore, by using the 3-D masterslice MMIC design approach proposed by the authors [8]–[10], we can greatly reduce development turn around time (TAT) and fabrication cost.

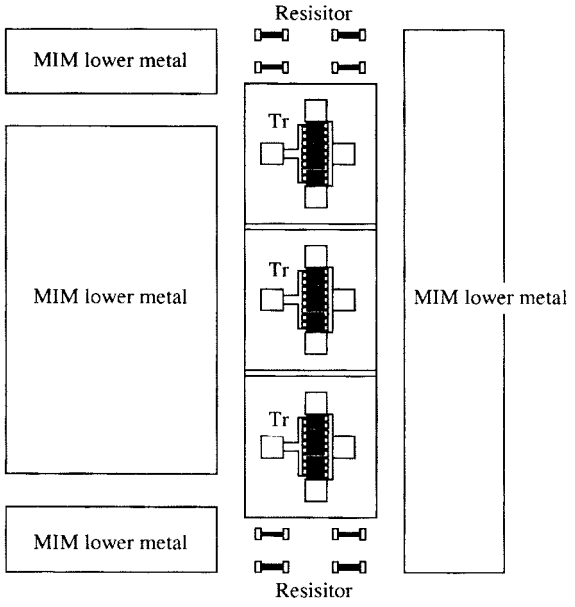
In this paper, the first monolithic 0.5-μm Si bipolar VCO's using 3-D MMIC technology are presented. After describing the structure and fabrication of the typical Si 3-D masterslice MMIC, we propose two Si VCO's with a very wide tuning range: one utilizes the varistor behavior of a transistor for controlling oscillation frequency; the other one utilizes a varactor diode. The former, a 5-GHz-band VCO MMIC [11], achieves the very wide tuning range of more than 33%; the ratio of the base–emitter conductance of the BJT can range from one to above eight. In addition, the oscillation frequency is linear against the base bias within the frequency tuning range. The measured phase noise is -83 dBc/Hz at 100 kHz and -110 dBc/Hz at 1-MHz offset from the carrier. To confirm the wide-tuning ability of the proposed VCO at higher frequencies, a 7-GHz-band VCO is designed and fabricated on the same Si masterslice array used for the 5-GHz-band unit. It achieves a 28% tuning range from 5.53 to 7.09 GHz at the collector bias of 2 V. The latter, a 6-GHz-band VCO whose frequency is controlled by a varactor diode, also offers a wide tuning range from 5.15 to 6.75 GHz at the collector bias of 3 V. The phase noise achieved ranges from -95 dBc/Hz to -117 dBc/Hz at 1-MHz offset frequency over the tuning range of 1.6 GHz (best phase-noise performance is -90.5 dBc/Hz at 100 kHz). The measured results confirm that the proposed Si VCO design can be realized at higher frequency. Furthermore, Si 3-D MMIC's are suitable for realizing lower cost, small chip size, and high-density integrated-circuit applications up to 30 GHz because Si BJT's have demonstrated that they can achieve $f_{\max}$ values of 70 GHz [12].

II. Structure and Fabrication

Fig. 1 shows the basic structure of the masterslice MMIC on an Si wafer. Many units, each of which contains BJT's, resistors, and the lower electrodes of metal–insulator–metal (MIM) capacitors, are used repeatedly to form a master array, and the whole wafer surface is passivated. The second-level metal



(a)



(b)

Fig. 1. Configuration of Si masterslice 3-D MMIC. (a) Cross-sectional view. (b) Array unit.

(Al), $GND1$, covers those elements not used in circuit design to form a ground plane. This metal simultaneously builds the different MIM capacitors such as shunt and series capacitors. The devices and first and second metal are manufactured using an ordinary Si integrated-circuit (IC) process. Next, thin-film polyimide layers and gold metal layers are stacked over the wafer and $GND1$ to complete the 3-D MMIC design. The fabrication process of the 3-D interconnection structure uses the folded metal interconnection technology (FMIT) with a thick insulator [6], almost the same as GaAs 3-D MMIC's. By allowing $GND1$ to cover a large part of the wafer, the conductive property of the wafer is effectively isolated from the passive structures built on and above $GND1$, and high Q passive circuits can be realized. In addition, the space for many miniature passive circuits can be created on $GND1$. $GND1$ (and/or an additional ground metal (Au), $GND2$, as occasion demands) and polyimide layers and metal layers provide passive circuits whose performance is not affected by the lossy Si substrate. Accordingly, the 3-D structure allows the use of reactive matching for monolithic Si circuit design which greatly improves the operating frequency of the Si MMIC's [8]. Furthermore, the 3-D masterslice MMIC technology reduces development TAT and fabrication cost.

III. Circuit Design

A. Basic Theory

The basic configuration of the first type of VCO is shown in Fig. 2(a). The VCO uses a series feedback topology with the BJT in common emitter configuration. The Si BJT is fabricated by 0.5-μm Super Self-Align Technology (SST1C's) [13]. Transistor size in the VCO is 0.3 μm $\times$ 13.4 μm $\times$ 9. Resistance R_1 (1 kΩ) is inserted between the base and control

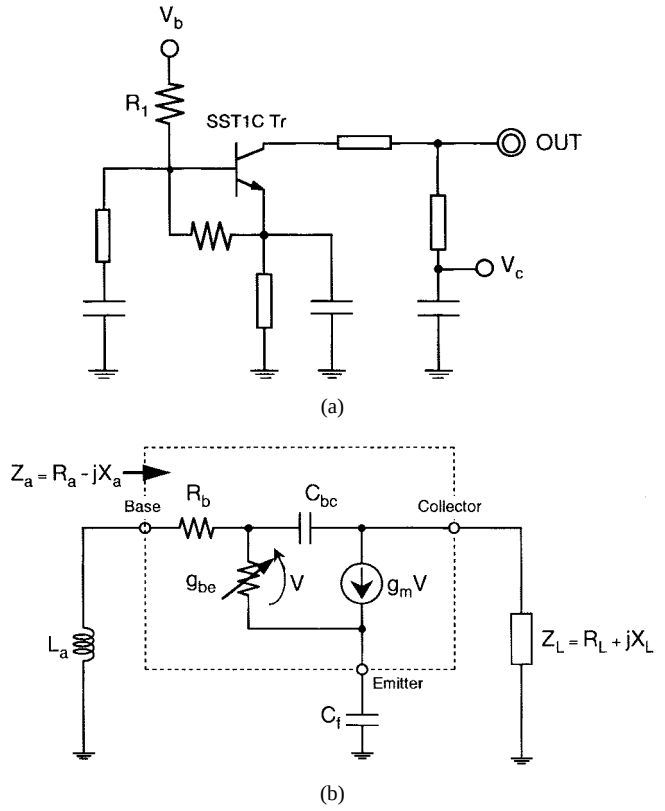


Fig. 2. Basic configuration of an Si BJT VCO. (a) Circuit schematic. (b) Equivalent circuit.

bias point so that the base current smoothly increases with control bias. The base is connected to the ground through a 40-Ω 30-μm-wide thin-film microstrip-line (TFMS) short-circuited stub [14]. The collector is connected to the VCO output port via a section of the TFMS line for impedance matching. Fig. 2(b) shows a simplified equivalent circuit for estimating frequency tuning performance of the proposed VCO, where R_b, $C_{\rm bc}$, $g_{\rm be}$, and g_m are the base resistance, the base-collector capacitance, the base–emitter conductance, and the transconductance of BJT, respectively. Voltages V_c and V_b are collector–base and control-base bias. The Y-matrix of the BJT (common-emitter BJT) is given below:

$$\begin{bmatrix} \dfrac{g_{\rm be}+j\omega C_{\rm bc}}{1+R_b(g_{\rm be}+j\omega C_{\rm bc})} & \dfrac{-j\omega C_{\rm bc}}{1+R_b(g_{\rm be}+j\omega C_{\rm bc})} \\ \dfrac{g_m-j\omega C_{\rm bc}}{1+R_b(g_{\rm be}+j\omega C_{\rm bc})} & \dfrac{j\omega C_{\rm bc}\{1+R_b(g_{\rm be}+g_m)\}}{1+R_b(g_{\rm be}+j\omega C_{\rm bc})} \end{bmatrix}. \tag{1}$$

From the Y-matrix (1), input impedance Z_a at the base [as shown in Fig. 2(a)] is obtained, as shown in (2), at the bottom of the page, where we can ignore capacitance C_f. If we focus on the base–emitter conductance $g_{\rm be}$ in (2), we obtain

$$\begin{aligned} Z_a &= R_a - jX_a \\ R_a &\propto \frac{a_1 g_{\rm be}^3 + a_2 g_{\rm be}^2 + a_3 g_{\rm be} + a_4}{(g_{\rm be}+g_m)(b_1 g_{\rm be}^2 + b_2 g_{\rm be} + b_3)} \\ X_a &\propto \frac{c_1}{b_1 g_{\rm be}^2 + b_2 g_{\rm be} + b_3} \end{aligned} \tag{3}$$

where, a_1, a_2, a_3, a_4, b_1, b_2, b_3, and c_1 are all constants. The above expressions show that the reactance X_a can be dynamically changed by the base–emitter conductance. Therefore, the oscillation frequency of the VCO using SST1C transistors is controlled by the base–emitter conductance, which depends on base current. Fig. 3 shows the base resistance R_b and the base–emitter conductance $g_{\rm be}$ of SST1C transistor as a function of base current. In Fig. 3, the values are normalized to the value at the standard current. The base–emitter conductance decreases in inverse proportion to the base current, where the base resistance is fixed. Thus, the base–emitter resistance works like a varistor with a ratio of one to more than eight. According to expression (3), the VCO can, by using the SST1C transistor, achieve a wide frequency tuning range without additional variable reactance elements such as varactors.

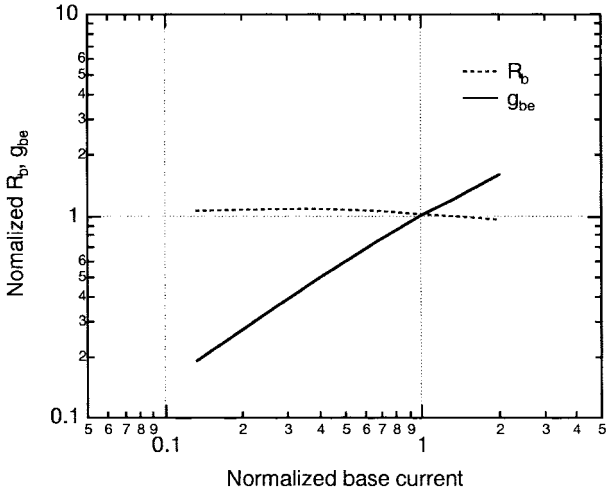


Fig. 3. Base resistance and base–emitter conductance of SST1C transistor as a function of base current.

The combination of using low-noise devices and raising the Q factor is effective for realizing a low phase-noise oscillator. As Si BJT's have lower noise than MESFET's and HEMT's at low frequencies, an Si BJT can be used to create a negative-resistance generator. However, this initial design does not consider the Q factor for estimating the original performance of Si 3-D MMIC VCO's, and uses the low-loss 40-Ω TFMS

$$\begin{aligned} Z_a = &-\frac{g_m\{g_{\rm be}+\omega C_{\rm bc}X_L(g_{\rm be}+g_m)\}+\omega^2C_{\rm bc}^2\{R_L(g_{\rm be}+g_m)-1\}-\{1+R_b(g_{\rm be}+g_m)\}\delta}{(g_{\rm be}+g_m)\delta} \\ &-j\frac{\omega C_{\rm bc}(g_mR_L-\omega C_{\rm bc}X_L-1)}{\delta} \\ \delta = &\{g_{\rm be}+\omega C_{\rm bc}X_L(g_{\rm be}+g_m)\}^2+\omega^2C_{\rm bc}^2\{R_L(g_{\rm be}+g_m)-1\}^2 \end{aligned} \tag{2}$$

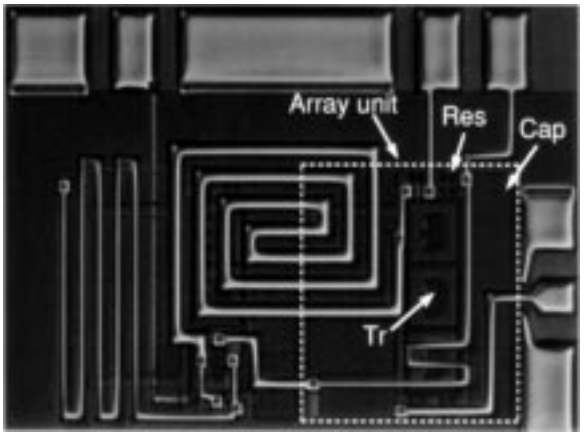


Fig. 4. Photograph of the fabricated 5-GHz-band Si bipolar VCO.

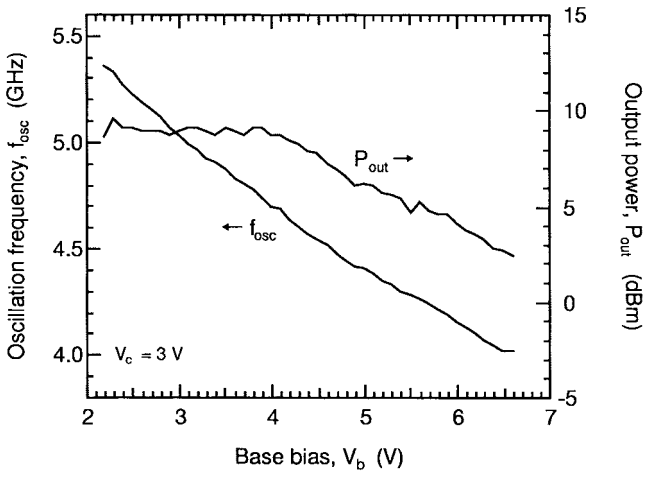
line as a resonator. Therefore, the loaded Q factor [15] of the 5-GHz-band VCO is only 0.58 and 0.59 at collector–bias levels of 1 V and 3 V, respectively. Raising the Q factor is a future technical subject.

B. Measured Performance

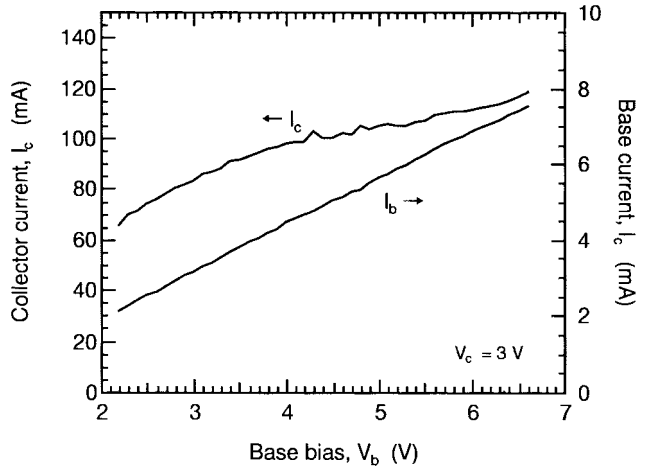
A microphotograph of the fabricated 5-GHz-band VCO MMIC chip is shown in Fig. 4. The total chip size prototype design is 1.3 $\times$ 0.9 mm^2; however, some of this area is consumed by unnecessary transistors, capacitors, and ground and RF probe pads because the VCO was manufactured on a masterslice Si substrate [8], [10]. The integrated VCO can be optimized to consume an area of less than 0.8 $\times$ 0.6 mm^2. The transistor's electrode and MIM capacitance bottom electrodes are connected to TFMS lines using via-holes. The 40-Ω 30-μm-wide TFMS line is formed in a spiral-like configuration, and its length is 3.66 mm for 5-GHz-band operation.

The oscillation frequency and output power as a function of base bias V_b are plotted in Fig. 5(a). The VCO achieves a very wide frequency tuning range from 4.02 to 5.35 GHz with output powers ranging from 2.3 to 8.5 dBm at the collector bias of 3 V. In addition, the linearity of oscillation frequency versus the controlled base bias is excellent within the tuning range. The high linearity of the proposed VCO is due to the linearity of base current versus control bias, as shown in Fig. 5(b). Utilizing the voltage dropping effect of resistor R_1, the VCO offers fine adjustment of the base voltage at the base of the BJT. We measured the tuning range versus base bias V_b for three different collector–bias values. The collector bias enhances the frequency tuning range and output power. At $V_c = 2$ V, a 30% tuning range is obtained; the output power ranges from -0.3 to 6.3 dBm. Even with the low dc-bias voltage of $V_c = 1$ V, it achieves 20% tuning range from 4.05 to 4.9 GHz and the frequency sensitivity of 820 MHz/V.

The phase noise of the VCO was directly measured using an HP8566B spectrum analyzer. The collector bias also basically enhances phase-noise characteristics because the collector current, whose standard value is 36 mA, increases. Fig. 6 shows the phase noise as a function of the offset frequency from center frequency. At $V_c = 3$ V and $V_b = 2.2$ V, the phase



(a)



(b)

Fig. 5. Performance of the 5-GHz-band VCO versus base bias V_b. (a) Frequency tuning range and output power. (b) Collector and base current.

noise is -83 dBc/Hz and -112 dBc/Hz at offset frequencies of 100 kHz and 1 MHz, respectively. Within the frequency tuning range, phase noise levels as low as -103 dBc at 1-MHz offset can be obtained, as shown in Fig. 6. As expected, phase noise increases with increasing base current (base bias V_b). This behavior corresponds to the increase of $1/f$ noise of BJT's with increasing base current.

C. Redesign of a 7-GHz-Band VCO

After measuring the 5-GHz-band VCO, we designed and fabricated a 7-GHz-band VCO to challenge higher frequency applications of the Si BJT oscillator. By utilizing the stock of the Si master array used for the 5-GHz-band VCO, we could save the Si IC process to complete the 7-GHz-band VCO. It takes only one month to manufacture the 7-GHz VCO after design. The prototype VCO also consists of a series feedback topology with the BJT in common emitter configuration to confirm the wide-tuning ability of the proposed VCO at higher frequencies. Fig. 7(a) shows photograph of the fabricated 7-GHz-band Si VCO. Difference between the 5- and 7-GHz-band VCO's is just TFMS line length. The 40-Ω TFMS line for a resonator is 1.61 mm long for the 7-GHz-band VCO.

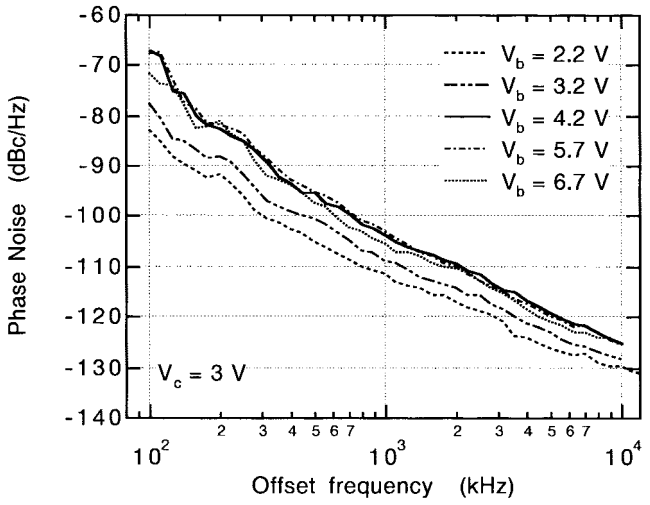
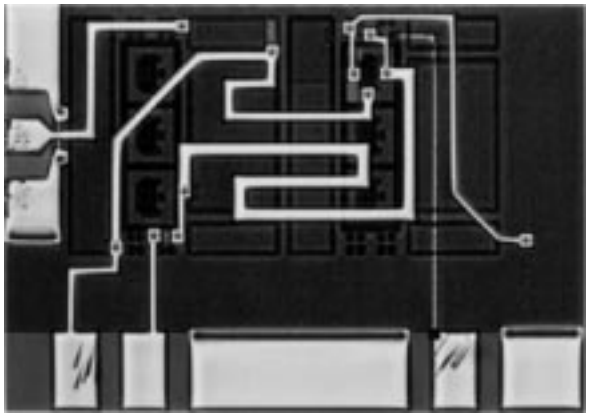


Fig. 6. Phase noise of the 5-GHz-band VCO at $V_b = 2.9$, 3.7, 5.0, 6.0, and 7.0 V.



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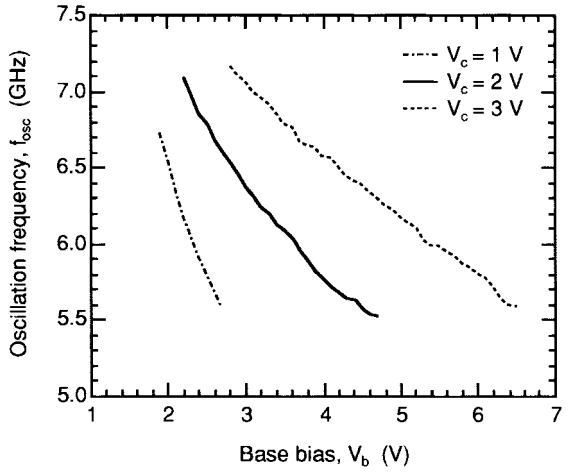
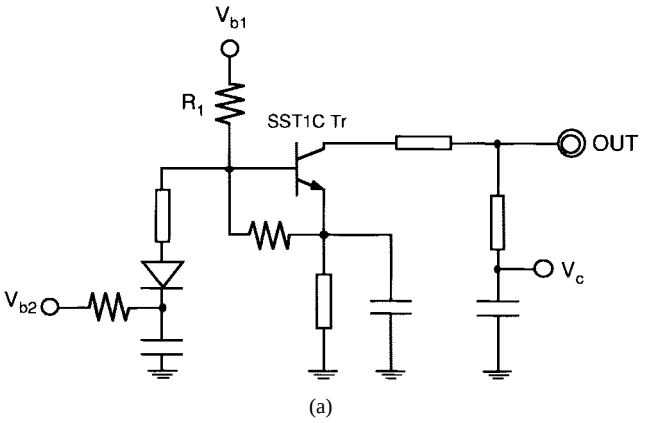


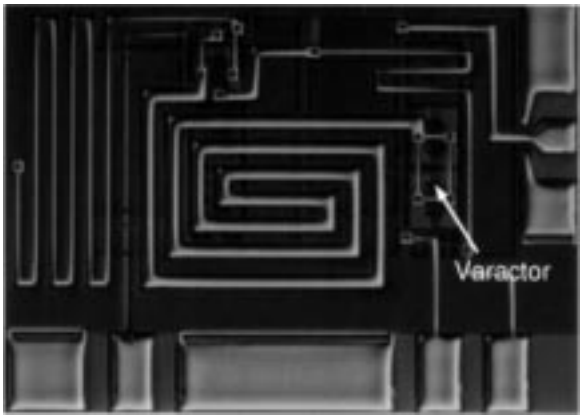
(b)

Fig. 7. A 7-GHz-band VCO fabricated on the same Si masterslice array used in constructing the 5-GHz-band one. (a) Photograph and (b) frequency tuning performance versus base bias V_b at $V_c = 1$, 2, and 3 V.

Fig. 7(b) shows the tuning range versus base bias V_b for three different collector–bias values. The 7-GHz-band VCO also achieves a wide tuning range because of varistor behavior. At $V_c = 2.0$ V, a 28% tuning range from 5.53 to 7.09 GHz is obtained; the output power ranges from 1.5 to 6 dBm. Even with the low dc-bias voltage of $V_c = 1$ V, the VCO achieves a 20% tuning range with control bias range between 1.9 and 2.7 V. Accordingly, the VCO achieves the high-frequency sensitivity of 1 GHz/V at $V_c = 1$ V. At $V_c = 3$ V, a 28% tuning range from 5.59 to 7.17 GHz is obtained; the output power ranges from 6 to 11.2 dBm. The measured phase-noise performance of the 7-GHz-band VCO is of the same order as that of 5-GHz-band device. At collector bias of 3 V, the 7-GHz-band VCO holds the phase noise under −102 dBc/Hz within the tuning range. The best phase noise is −86.5 dBc/Hz at 100-kHz offset and −113 dBc/Hz at 1-MHz offset from the carrier. The measured results confirm that the proposed Si VCO is suitable for realizing microwave oscillators with wide tuning range.



(a)



(b)

Fig. 8. (a) Circuit schematic and (b) photograph of a 6-GHz-band VCO using a varactor diode.

IV. VCO WITH A VARACTOR

We also designed another VCO with a varactor diode for evaluating varactor-diode application to Si 3-D MMIC oscillators. Fig. 8(a) shows a circuit schematic of this VCO, where V_c, V_{b1}, and V_{b2} are collector bias, base bias of the transistor generating negative resistance, and control bias of the varactor diode, respectively. A varactor utilizing the base–collector junction, i.e., the base–collector capacitance C_{bc} of a transistor is inserted in the resonant tank connected to the base of the BJT. The base–collector capacitance tuning

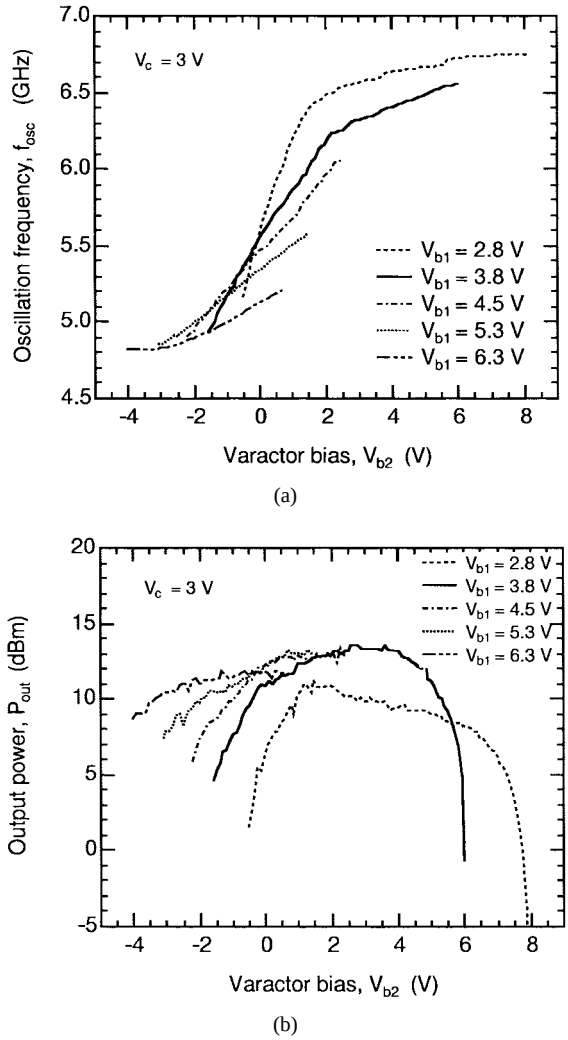


Fig. 9. (a) Frequency tuning performance and (b) output power of the 6-GHz-band VCO as a function of varactor bias V_{b2} at $V_c = 1$, 2, and 3 V.

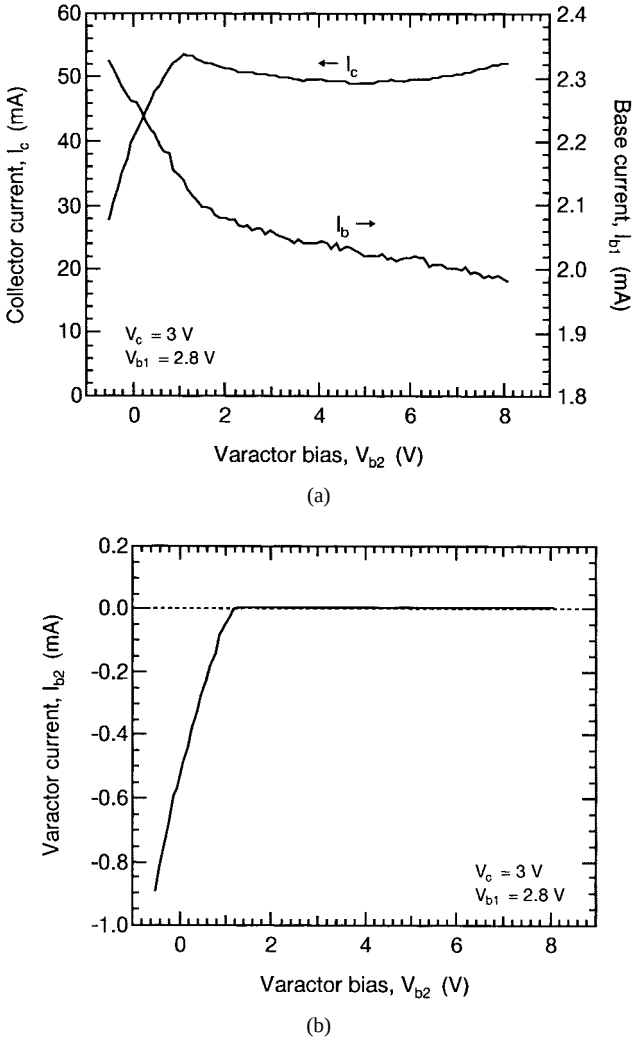


Fig. 10. Collector current (a) I_c, base current I_{b1}, and (b) varactor current I_{b2} of the VCO as a function of the varactor bias V_{b2}.

performance depends on collector–base bias $V_{\rm cb}$. The tuning capacitance ratio is 1.7:1 from 0 to -2 V for the 0.3 μm $\times$ 13.4 μm $\times$ 9 unit transistor. The loaded Q factor of the 6-GHz-band VCO is 0.63 at the collector bias of 1 V, as low as that of the 5-GHz-band VCO shown in Fig. 2(a). Fig. 8(b) shows a microphotograph of the fabricated 6-GHz-band MMIC VCO. The intrinsic chip size is 1 $\times$ 0.65 mm^2, and the varactor is used by connecting two unit transistors. The 40-Ω 30-μm-wide TFMS line is formed in a spiral-like configuration, and its length is 4.18 mm for a 6-GHz-band.

Fig. 9 shows frequency tuning range and output power of the 6-GHz-band VCO as a function of control bias V_{b2} for V_{b1} values of 2.8, 3.8, 4.5, 5.3, and 6.3 V. Tuning range and frequency sensitivity greatly depend on the base bias V_{b1}. At $V_{b1} = 3.8$ V, the VCO exhibits the widest tuning range (33%) from 4.93 to 6.55 GHz. While the tuning range is only 8% at $V_{b1} = 6.3$ V. In addition, we can obtain variable frequency sensitivity from 130 to 870 MHz/V by the base bias. This is because the varistor and varactor have opposite effect on oscillation frequency tuning. We explain this using Fig. 10, which plots the different current values versus the varactor bias V_{b2}. At $V_{b1} = 1.2$ V, the varactor diode current I_{b2} begins to flow from base to collector, as shown in Fig. 9(b), resulting in an increase in the base current I_{b1}. Therefore, the base voltage at the base of the transistor decreases due to the increase in voltage drop caused by R_1. The collector current behavior, shown in Fig. 9(a), corresponds to this decrease in base voltage. According to the results in Fig. 5, the oscillation frequency goes up as the collector current falls. However, the frequency of the 6-GHz-band VCO becomes low because of the varactor behavior. This shows that the varistor and varactor effect have opposite tuning effects. Turning over the varactor electrode is one of the most simple and effective solutions to this problem. In addition, it is possible to achieve much wider frequency tuning range.

Fig. 11 shows the phase noise of the VCO as a function of varactor bias at the collector bias of 3 V. The measured phase noise level is as low as -105 dBc/Hz at 1-MHz offset frequency with varactor bias levels from -0.25 V to 8 V. Below $V_{b2} = 1.5$ V, the phase noise increases with increasing capacitance nonlinearity of the varactor diode. Using a pair of varactors antidirectionally coupled in series will solve this problem because each varactor cancels the capacitance nonlinearity of the other [15]. Fig. 12 shows the

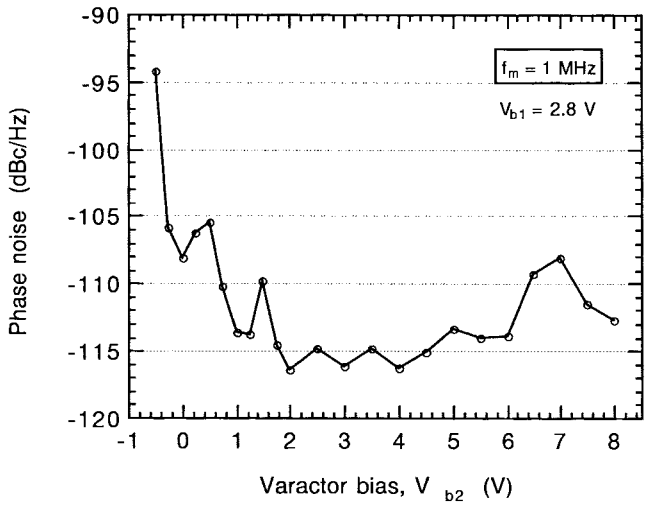
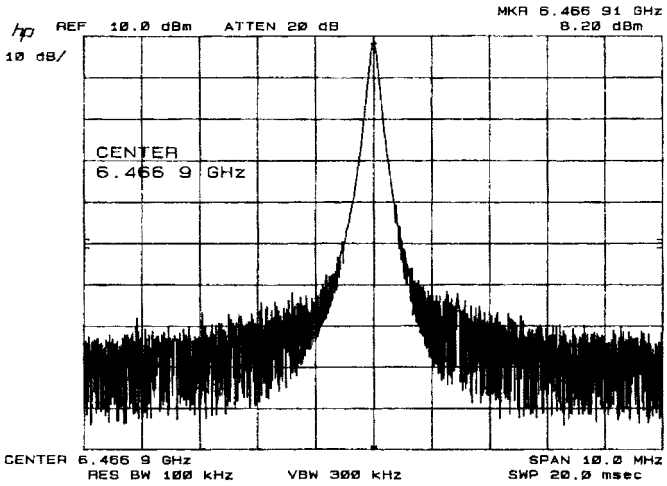
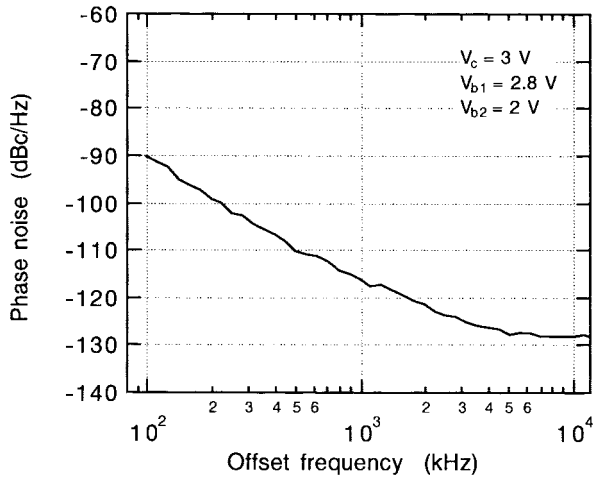


Fig. 11. Oscillation output spectrum and phase noise versus offset frequency of the 6-GHz-band VCO at $V_c = 3$ V, $V_{b1} = 2.8$ V, and $V_{b2} = 2$ V.



(a)



(b)

Fig. 12. Phase noise at 1-MHz offset frequency of the 6-GHz-band VCO as a function of varactor bias, V_{b2}. (a) Output spectrum. (b) Phase noise performance.

output spectrum and phase-noise characteristic versus offset frequency of one measured oscillator. Bias conditions are $V_c = 3$ V, $V_{b1} = 2.8$ V, and $V_{b2} = 2$ V. The VCO oscillates at 6.47 GHz with the output power of 9.7 dBm. The phase noise is -90.5 dBc/Hz at 100-kHz offset and -116.4 dBc/Hz at 1-MHz offset from the center carrier.

V. Conclusion

The first prototype VCO's based on 3-D MMIC's have been constructed using 0.5-μm Si BJT technology. The fabricated 5-GHz-band VCO' offers a very wide tuning range (33%) and highly linear oscillation frequency. We also demonstrated a 7-GHz-band VCO to show the wide tuning ability of the proposed VCO at higher frequencies. That VCO, constructed on a master array, also achieves a 28% tuning range. The phase noise offered by a 6-GHz-band VCO that uses a varactor diode is -90.5 dBc/Hz at 100 kHz and -116.4 dBc/Hz at 1-MHz offset from the carrier. The measured results described herein make Si 3-D MMIC VCO's attractive candidates for low-cost low phase noise, and wide tuning oscillators for microwave frequency applications.

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